ECR #: 41
Title: Clarification of Point to Point A.G.P.
Release Date: 12/18/97
Impact: Clarification
Spec Version: A.G.P. 1.0

Summary: Some have interpreted the A.G.P. specification to mean that only two devices can reside on the A.G.P. interface. The specification should not require this, but allow the system designer to implement different topologies as long as the system meets the requirements specified in the A.G.P. specification.

Background: The A.G.P. specification specifies communication between two agents, one being a master and the other a target. The current specification has been interpreted to mean that only two devices can reside on the interface. This would mean that if the graphics device is on the motherboard, then no add-in capability can exist. However, the specification should not preclude a system designer from developing a system that allows a graphics device to be on the motherboard and provide an upgrade via the A.G.P. connector. When this is done, the motherboard device must be disabled when the add-in card is present. However, the requirement remains that communication is between only one master and one target on the interface.

Change Current Specification as shown:

(Page numbers, sections, etc., refer to A.P.G. Specification Revision 1.0 - dated July 31, 1996)

Page 7, Section 2.4, First bullet after Paragraph 1

CURRENT Text:

- The A.G.P. is a point-to-point connection, intended for use by a 3D graphics accelerator only, and, …

CHANGE:

- The A.G.P. is a point to point[1] connection, intended for use by a 3D graphics accelerator only, and,

[1] This means that active communication can only occur between two A.G.P. agents that reside on the interface, where one agent is referred to as the A.G.P. target and the other the A.G.P. master. The simplest implementation is to only have two devices attached to the bus. Attaching more than two devices to the interface is not precluded as long as there is only one active master and one active target. Any other device must not respond to or interfere with the interface operation. When more than two devices are attached to the interface, the system designer is responsible to ensure that all requirements of this specification are met, since the component and/or add-in card designer has no control how the devices are used.

Page 85, Section 4.3.5, Paragraph 1, Sentence 1, 2 in Rev. 1.0:

CURRENT:
The AC timings and electrical loading on the A.G.P. interface are optimized for one host component on the motherboard and one A.G.P. compliant agent either on the motherboard or through a connector. The interface is a point to point network with a maximum electrical length of 3 ns.

CHANGE:
The AC timings and electrical loading on the A.G.P. interface are optimized for one active host component on the motherboard and one active A.G.P. compliant agent either on the motherboard or through a connector. The interface is a logical point to point[2] network with a maximum electrical length of 2.5 ns. If a bus with more than two loads and/or branching in the topology is implemented, it is the system designers responsibility to ensure compliance to this specification. This can be accomplished by thoroughly simulating the design to ensure proper signal quality and timings are met. These topologies are not shown or discussed in this specification due to the difficulty in designing them and it is recommended that a physical point to point topology be used.

[2] See footnote 1, page 7.

New information for Rev. 2.0:

Page 175, Section 4.3.1:

CURRENT:
The AC timings and electrical loading on the A.G.P. interface are optimized for one host component on the motherboard and one A.G.P. agent either on the motherboard or through a connector. The interface is a point to point network. The board routing should use layout design rules consistent with high speed digital design. Due to the high speed nature of the A.G.P. bus, any design should be thoroughly simulated and every effort should be made to reduce signal skew and improve signal quality.

CHANGE:
The AC timings and electrical loading on the A.G.P. interface are optimized for one active host component on the motherboard and one active A.G.P. agent either on the motherboard or through a connector. The interface is a logical point to point[3] network. The board routing should use layout design rules consistent with high speed digital design. Due to the high speed nature of the A.G.P. bus, any design should be thoroughly simulated and every effort should be made to reduce signal skew and improve signal quality. If a bus with more than two loads and/or branching in the topology is implemented, it is the system designers responsibility to ensure compliance to this specification. This can be accomplished by thoroughly simulating the design to ensure proper signal quality and that the timings are met. These topologies are not shown or discussed in this specification due to the difficulty in designing them, especially at the higher transfer rates, and it is recommended that a physical point to point topology be used.

[3] See footnote 1, page 7.

Page 189, Section 4.4.5.3:

CURRENT:
The AC timings and electrical loading on the A.G.P. interface are optimized for one host component on the motherboard and one A.G.P. agent either on the motherboard or through a connector. The interface is a point to point network, with a maximum electrical length of 2.5 ns. The board routing should use layout design rules consistent with high speed digital design. Due to the high speed nature of the A.G.P. bus, any design should be thoroughly simulated and every effort should be made to reduce signal skew and improve signal quality. The following paragraphs summarize the board layout restrictions on the 2X transfer mode interface.

CHANGE:
The AC timings and electrical loading on the A.G.P. interface are optimized for one active host component on the motherboard and one active A.G.P. agent either on the motherboard or through a connector. The interface is a logical point to point network, with a maximum electrical length of 2.5 ns. The board routing should use layout design rules consistent with high speed digital design. Due to the high speed nature of the A.G.P. bus, any design should be thoroughly simulated and every effort should be made to reduce signal skew and improve signal quality. If a bus with more than two loads and/or branching in the topology is implemented, it is the system designers responsibility to ensure compliance to this specification. This can be accomplished by thoroughly simulating the design to ensure proper signal quality and that the timings are met. These topologies are not shown or discussed in this specification due to the difficulty in designing them and it is recommended that a physical point to point topology be used. The following paragraphs summarize the board layout restrictions on the 2X transfer mode interface.